Atty Docket No.: JCLA6968 Serial No.: 09/838,752

REMARKS

Present Status of the Application

The Office Action dated August 26, 2002 rejected claim 6 under 35 USC 102(b) as being anticipated by Raiser et al. (US Patent No. 6,049,124), and claims 1, 4, 6, 9, 12, 14, and 17 under 35 USC 102(e) as being anticipated by Farnworth (US Patent No. 6,252,302). Claims 2, 3, 5, 7, 8, 10, 11, 13, 15, 16, and 18 were further rejected under 35 USC 103(a) as being unpatentable over Farnworth. Furthermore, claims 1-5 and 9-18 were rejected under 35 USC 112, second paragraph, as being indefinite for containing elements that lack clear antecedent basis. The drawings were also objected to for failing to show elements (i.e. "the other chips") recited in the claims.

The Applicants have most respectfully considered the remarks set forth in the Office Action. Claims 1-8 have been cancelled, and claims 9 and 14 have been amended to comply with 35 USC 112. For at least the reasons discussed hereafter, its is respectfully submitted that all the claims 9-18, now pending in the application, are patently distinguish over the above cited references. Reconsideration of the claims therefore is earnestly requested.

Discussion of the Claim Rejections

Claim rejection under 35 USC 112

The Office Action rejected claims 1-5 and 9-18 under 35 USC 112, second paragraph, as being indefinite for containing elements that lack clear antecedent basis.

As set forth above, claims 9 and 14 have been amended into a proper form that the Applicants believe to comply with the requirement of claim language definiteness. Accordingly,

withdrawal of the rejection is respectfully requested.

The Applicants notice that the drawings properly show a plurality of chips 304, 404 are stacked on one another on the die pad 306 as recited in amended claim 9. It is therefore respectfully submitted the objection to the drawings is moot, the withdrawal of which is respectfully requested.

Claim rejection under 35 USC 102

The Office Action rejected claim 6 under 35 USC 102(b) as being anticipated by Raiser et al. and claims 1, 4, 6, 9, 12, 14, and 17 under 35 USC 102(e) as being anticipated by Farnworth. Since claims 1-8 have been cancelled as set forth in the above amendments, the present discussion therefore will only focus on claims 9, 12, 14, and 17, the rejection of which is respectfully traversed.

As described in claim 9 (and also in claim 14), the invention teaches a package of semiconductor device that comprises a die pad, a plurality of leads, and a chip including an active surface with beveled edges and a back surface attached to the die pad via an adhesive material. The adhesive material covers the whole back surface of the chip and the side surfaces of the chip that connect its back surface to its active surface. As disclosed on, for example, page 6:lines 8-10 of the specification, the provision of beveled edges favorably prevents a coverage of the active surface of the chip by an overflowed adhesive material.

Neither Farnworth nor Raiser et al. teach or suggest the claimed invention as described above.

Farnworth discloses a chip 76 (referred to as die/dice in the patent) that may be illustrated as

having an active surface with a beveled edge (FIG 4&6), but this feature is not referred to anywhere in the written description. Furthermore, the known package structure is constructed from an encapsulation device 45 in a chamber 55 of which the chip 76 is inserted and electrically connected via a spring portion 86 (see col. 3: 51-67), a cap 70 with a compression pad 130 further sealing the chamber 55. This disclosure substantially differs from that of the invention as recited in claim 9 (and claim 14) and discussed above.

Raiser et al. may disclose a semiconductor package in which a chip 310 also has an active surface 316 provided with a beveled edge 512 (see col. 5: 1-10 & FIG 4). However, the described package structure does not have a chip mounted on a die pad with an adhesive material attaching the back surface of the chip to the die pad, as recited in claims 9 and 14. Nor Raiser et al. describes the active surface of the chip is electrically connected to a plurality of leads through wires. Instead, the chip of Raiser et al. is attached on the substrate 412 through its active surface 316, and is further electrically connected via a plurality of solder connections 318 formed on the active surface 316. In addition to the above distinguishable claim features, claim 14 further discloses the stack of a plurality of chips on one another on the die pad, which is not disclosed and suggested in any of the references discussed in the Office Action.

For at least the above reasons, it is therefore respectfully submitted that the invention as a whole, as recited in claims 9 and 19, patently distinguishes over the cited references, and the withdrawal of the rejection is respectfully requested. Claims 12 and 17 should be also patentable by virtue of their respective dependency upon patentable claims 9 and 14.

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Claim rejection under 35 USC 103

The Office Action rejected claims 2, 3, 5, 7, 8, 10, 11, 13, 15, 16, and 18 under 35 USC 103(a) as being allegedly unpatentable over Farnworth. This rejection is respectfully traversed.

For at least the reasons that claims 10, 11, 13, 15, 16, and 18 are dependent upon claims 9 and 14 that, as discussed above, patentable over the cited references, it is however submitted that these claims should be patentable over the cited references. Withdrawal of the rejection is therefore respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 9-18 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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VERSION WITH MARKED-UP AMENDMENTS TO SHOW THE CHANGES MADE

In The Claims:

The claims have been amended as follows.

9. (Once amended) A package of a semiconductor device, the package comprising:

a carrier, having a die pad and a plurality of leads;

a chip, located on a surface of the die pad, wherein the chip has an active surface and a corresponding back surface that are connected to each other via a plurality of side surfaces, wherein the active surface has beveled edges;

an adhesive material, [that adheres] attaching the back surface of the chip to the surface of the die pad, wherein the adhesive material covers the whole back surface of the chip and [around] the [sides] side surfaces of the chip, the beveled edges of the active surface preventing a coverage of the active surface by the adhesive material;

a plurality of wires, [that] electrically connecting the [nodes] leads of the carrier to the active surface of the chip; and

a molding compound, [that covers] covering the chip, the wires and a portion of the leads.

14. (Once amended) A package of a semiconductor device, the package comprising:

a carrier, having a die pad and a plurality of leads;

a plurality of chips, [wherein one of chips is located on a top surface of the die pad and the other chips are stacked on each other,] each chip [has] having an active surface and a corresponding back surface that are connected to each other via a plurality of side surfaces, and the active surface has beveled edges, wherein the chips are stacked on one another on the die pad in such a manner that the active surface of one chip faces the back surface of one chip adjacently stacked thereon;

an adhesive material, [that fills in between each chip and a space between the top surface of the die pad and one of the back surfaces of the chips] respectively attaching the chips to one another and to the die pad, wherein the adhesive material respectively covers the whole back

surface and [both sides] the side surfaces of the chips, the beveled edges preventing a coverage of the corresponding active surfaces by the adhesive material;

a plurality of wires, [that] electrically connecting [to] the [nodes] leads of the carrier to the respective active surfaces of the chips; and

a molding compound, [that covers] covering the chips, the wires and a portion of the leads.